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APPLICATION N	10.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/042,733		10/25/2000	Curtis Priem	18659-15C1	8456
23419	75	90 03/01/2005		EXAMINER	
		DWARD, LLP	TUNG, KEE M		
• • • • • • • • • • • • • • • • • • • •		NO REAL SQUARE	ART UNIT	PAPER NUMBER	
		CA 94306	2676		
				DATE MAILED: 03/01/2005	

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(a)					
		Applicant(s)					
Office Action Summary	10/042,733	PRIEM ET AL.					
Office Action Guilliary	Examiner	Art Unit					
	Kee M Tung	2676					
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply							
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).							
Status							
1) Responsive to communication(s) filed on 05 No	ovember 2004.						
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· <u> </u>	· <u> </u>						
·— · · ·	closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims							
4)⊠ Claim(s) <u>25-44</u> is/are pending in the application.							
	4a) Of the above claim(s) is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.							
6)⊠ Claim(s) <u>25-44</u> is/are rejected.							
7) Claim(s) is/are objected to.							
8) Claim(s) are subject to restriction and/or	election requirement.						
Application Papers							
9)☐ The specification is objected to by the Examiner							
10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.85(a).							
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.							
Priority under 35 U.S.C. § 119							
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 							
3. Copies of the certified copies of the priority documents have been received in this National Stage							
application from the International Bureau (PCT Rule 17.2(a)).							
* See the attached detailed Office action for a list of the certified copies not received.							
Attachment(s)							
1) Notice of References Cited (PTO-892)	4) Interview Summary						
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) 	Paper No(s)/Mail Da 5) Notice of Informal P	ite atent Application (PTO-152)					
Paper No(s)/Mail Date	6) Other:	a.c , ppilodeon (1 10-102)					

Application/Control Number: 10/042,733

Art Unit: 2676

DETAILED ACTION

The amendment filed 11/5/04 has been considered in preparing this Office action.

Claim Rejections - 35 USC § 103

- 1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 2. Claims 25-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Porterfield (6,069,638) in view of Morgan et al (5,821,940 hereinafter "Morgan").

Porterfield teaches a graphics system (Fig. 1) comprising an I/O bus (PCI bus 108); a CPU (102) having an associated system memory (106), said CPU and said associated system memory coupled to said I/O bus, said CPU adapted to issue commands for rendering polygons of a graphical image; a graphics accelerator (110) coupled to said I/O bus. However, Porterfield fails to explicitly teach the details of the graphics accelerator comprising a cache and a cache controller. These are what Morgan teaches. Morgan teaches a graphics system (Fig. 5) comprising a CPU (12) having an associated system memory (not shown, but is inherent by any computer, furthermore, Morgan teaches display list memory is portion of the system memory, col. 3, lines 51-54), the details of the graphics accelerator (the combination of display list controller 16, transformation processor 18, cache storage means 22 and backend processor 24) comprising a cache (28) for storing vertex data; a cache controller (26) configured to receive a command to render a polygon from said CPU, said cache

Application/Control Number: 10/042,733

Art Unit: 2676

controller (26) checking said cache (28) for previously cached vertex data for vertices of said polygon; and said graphics accelerator configured to utilize said vertex data to render pixel data for said polygon; wherein said graphics accelerator caches vertex data received from said I/O bus to reduce the number of data transfers of vertex data across said I/O bus required to render polygons in response to said commands issued from said CPU. Therefore, it would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the detailed teachings of graphics accelerator with cache into the graphics accelerator of Porterfield in order to reduce memory access bandwidth from system memory over the I/O bus and thus will help to increase overall system performance. Therefore, at least claim 25 would have been obvious by Morgan.

Page 3

As per claim 26, Morgan fails to explicitly teach a state machine for directing said cache controller to update said cache. It is noted that a state machine is considered an old and well know feature for the CPU to include. Therefore, claim 26 would have been obvious.

As per claims 30-33 and 36, Porterfield further teaches a DMA engine for transferring vertex data from main memory to local memory (162) in DMA model 9col. 7, lines 2-8).

As per claims 34 and 35, Porterfield teaches said CPU is coupled to say I/O bus by a graphics bridge and said system memory is connected to said graphics bridge (Fig. 3).

Method claim 37 is similar in scope to system claim 25, and additionally requires index values of cache for vertex data of said vertices of said polygon (col. 3, lines 35-43). Therefore, at least claims 27 and 37 would have been obvious.

Method claim 41 is similar in scope to system claim 25 and method claim 37, and additionally requires performing a memory transfer operation to transfer required vertex data from system memory (from display list memory 14, col. 3, lines 20-43) to cache. Morgan further teaches performing a memory transfer operation to transfer required vertex data from display list memory (14) to cache memory (28). Therefore, at least claims 28-29 and 38-44 would have been obvious.

Response to Arguments

3. Applicant's arguments with respect to claims 25-44 have been considered but are moot in view of the new ground(s) of rejection.

The rejections have been modified in order to fully considered applicant's amendment and arguments.

Regarding applicant's arguments of bus 31 of Morgan as an I/O bus, it is noted that since the combination of display list controller 16, transformation processor 18, cache storage means 22 and backend processor 24 are considered as the graphics accelerator, thus, the internal bus of 31 can not be the I/O bus and the back end processor 24 is just part of the graphics accelerator.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

Art Unit: 2676

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kee M Tung whose telephone number is 703-305-9660. The examiner can normally be reached on Tuesday - Friday from 5:30 am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Application/Control Number: 10/042,733 Page 6

Art Unit: 2676

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kee M Tung

Primary Examiner

Art Unit 2676